

REMARKS

The Office Action dated January 9, 2006, has been received and carefully noted. The above amendments to the claims, and following remarks, are submitted as a full and complete response thereto.

Claims 1-21 are currently pending, of which claims 1, 7, 13, and 16 are independent claims. Claims 13, 16, and 19 have been amended to more particularly point out and distinctly claim the invention. No new matter has been added. In view of the remarks that follow, claims 1-21 are respectfully submitted for consideration.

Claims 7-12 were rejected under 35 U.S.C. 112 as being indefinite because claim 7, upon which claims 8-12 depend, recites “a table means,” “a cache means,” and “a search engine means.” Similar “means” language in claim 8 is objected to for the same reason. The Office Action asserts that it is not clear what structures those terms reference.

Applicant respectfully notes that Figure 4 and paragraph 0038 of the present application provide some example structure. For example, the described 60 bit wide, 128 entry cache is an example embodiment of the cache means. The described 16K table is an example embodiment of the table means. The described search stage zero is an example embodiment of the search stage zero segment means. The described search stage one is an example embodiment of the search stage one segment means. The combined described search stage zero and search stage one are an example embodiment of the search engine means. As discussed in paragraph 0055 of the present application,

the present invention can be embodied on a semiconductor substrate, such as silicon, with appropriate semiconductor manufacturing techniques based on a circuit layout. In view of the illustrative description in the specification, it is respectfully submitted that the features identified by the Office Action are definite. Therefore, it is respectfully requested that this rejection be withdrawn.

Claims 1, 7, 13, and 16 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,414,704 of Spinney ("Spinney"). Applicants respectfully traverse this rejection.

Claim 1, upon which claims 2-6 depend, is directed to a table search device. The device includes a table having a plurality of entries. The device also includes a cache having a subset of entries of the plurality of entries of the table. The device further includes a search engine configured to first search the cache in a first number of search cycles and then search the table in a second number of search cycles based on search results of the cache. The search engine is connected to the table and the cache.

Claim 7, upon which claims 8-12 depend, is directed to a table search system. The table search system includes a table means for storing a plurality of entries. The table search system also includes a cache for storing a subset of entries of the plurality of entries of the table means. The table search system further includes a search engine means for initially search the cache means in a first number of search cycles and then searching the table means in a second number of search cycles based on search results of the cache means.

Claim 13, upon which claims 14-15 depend, is directed to a method for performing a table lookup. The method includes creating a table having a plurality of entries. The method also includes creating a cache having a subset of entries of the plurality of entries of the table. The method further includes searching, by a search engine, the cache in a first number of search cycles. The method additionally includes searching, by the search engine, the table in a second number of search cycles based on search results of the cache.

Claim 16, upon which claims 17-21 depend, is directed to a network switch. The network switch includes an ARL table having a plurality of entries. The network switch also includes an ARL cache having a subset of entries of the plurality of entries of the ARL table. The network switch further includes a search engine configured to first search the ARL cache in a first number of search cycles and then search the ARL table in a second number of search cycles based on search results of the ARL cache. The search engine is connected to the ARL table and the ARL cache.

It is respectfully asserted that the cited art of Spinney does not disclose or suggest all of the elements of any of the presently pending claims.

Spinney is directed to address lookup in a packet data communications link, using hashing and content-addressable memory. Spinney aims to provide address translation in a system without any additional overhead. More specifically, Spinney was trying to provide address translation while minimizing space needed on a printed circuit board,

cost, and electrical consumption. Additionally, Spinney wanted to avoid adding additional chips to the already required chips.

Claim 1 recites “a cache having a subset of entries of said plurality of entries of said table.” Spinney does not disclose or suggest at least this feature of the invention. In Spinney, a CAM memory chip can in certain embodiments contain a single address. However, as explained at col. 3, ll. 22-35, this only occurs when more than seven 48-bit addresses bit addresses hash to the same address. Moreover, as explained by Spinney, the address is not copied to the CAM memory chip, but placed there. The reason why it is placed there is evident. There is no place for it within the bucketed system. Accordingly, in Spinney even assuming that the CAM memory chip were a cache (which is not how Spinney describes it), the CAM memory chip does not have a subset of entries (plural) of said plurality of entries of said table. Accordingly, it is respectfully submitted that Spinney does not disclose all of the elements of claim 1. Therefore, it is respectfully requested that the rejection be withdrawn.

Claims 7, 13, and 16 recite similar limitations, and thus the same arguments as applied to claim 1 apply to claims 7, 13, and 16, although the scopes of those claims differ from the scope of claim 1: “a cache means for storing a subset of entries of said plurality of entries of said table means” (claim 7), “creating a cache having a subset of entries of said plurality of entries of said table” (claim 13), and “an ARL cache having a subset of entries of said plurality of entries of said ARL table.”

Claims 3-4, 9-10, 14-15, and 18-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Spinney in view of no other references. The Office Action takes the position that it would have been obvious to modify Spinney such that claims 3, 4, 9, 10, 14, 15, 18, and 19 would read on it. Applicants respectfully traverse this rejection.

Claims 3-4 depend from claim 1, claims 9-10 depend from claim 7, claims 14-15 depend from claim 13, and claims 18-19 depend from claim 16. As explained above, Spinney fails to disclose or suggest all of the elements of claims 1, 7, 13, and 16. Accordingly, Spinney fails to disclose or suggest all of the elements of claims 3-4, 9-10, 14-15, and 18-19.

Although the Office Action suggests that it would have been obvious to modify Spinney in certain respects, it is respectfully submitted that those modifications are moot in view of the other deficiencies of Spinney as identified above. It would not have been obvious to modify Spinney to remedy the above-identified deficiencies. Accordingly, it is respectfully submitted that claims 3-4, 9-10, 14-15, and 18-19 are not obvious in view of Spinney. It is therefore respectfully requested that this rejection be withdrawn.

Claims 2, 5, 6, 8, 11, 12, 17, 20, and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Spinney in view of U.S. Patent No. 6,453,358 of Michels et al. (“Michels”). The Office Action takes the position that Spinney teaches most of the elements of the claims, and supplies Michels to remedy Spinney’s deficiencies. Applicants respectfully traverse this rejection.

Claims 2, 5, and 6 depend from claim 1, claims 8, 11, and 12 depend from claim 7, and claims 17, 20 and 21 depend from claim 16. As explained above, Spinney fails to disclose or suggest all of the elements of claims 1, 7, 13, and 16. Accordingly, Spinney fails to disclose or suggest all of the elements of claims 2, 5, 6, 8, 11, 12, 17, 20, and 21. However, the Office Action supplies Michels in an attempt to remedy the deficiencies of Spinney.

It is respectfully suggested that the combination of Spinney and Michels does not disclose or suggest all of the elements of any of the presently pending claims.

Spinney is discussed above. Michels is directed to a network switching device with concurrent key lookups. The switching device includes multiple binary search engines coupled in series including one or more precursor search engines, and a final stage binary search engine. Michels states that it uses pipelining, which it defines as connecting search engines in series. Michels asserts that by pipelining search engines, increased throughput can be achieved. Michels posits that it is another aspect of Michels' invention to permit each of the search engines to perform concurrent source and destination searches of the lookup table.

Michels does not remedy the deficiencies of Spinney, because Michels does not suggest modifying a CAM memory such as Spinney provides such that the CAM memory would become "a cache having a subset of entries of said plurality of entries of said table." Instead Michels proposes a search system that employs multiple stages. A first stage memory (which Michels does not describe as a cache) contains a subset of

Michels lookup table. Michels first stage memory is nothing like Spinney's CAM memory, except that both are memories. Accordingly, Michels does not remedy the deficiencies of Spinney, because Michels does not disclose or suggest modifying Spinney's to include "a cache having a subset of entries of said plurality of entries of said table."

The Office Action suggests that one of ordinary skill in the art would combine Michels and Spinney to perform the address lookup of Michels using separate search stages. It is respectfully submitted that this suggested motivation to combine is flawed. As noted above, Spinney is concentrated on providing address lookup while minimizing cost, energy usage, and circuit board space. It is respectfully submitted that Michels separate search stages (with corresponding separate search engines) would necessarily require more circuit board space, and increase cost.

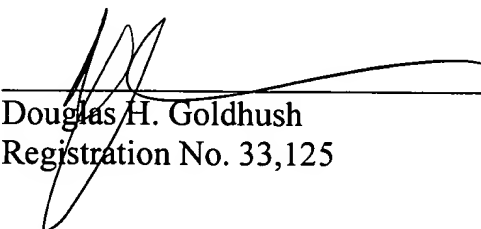
Although the Office Action suggest that Michels would improve the speed of operation of Spinney, it is respectfully noted that Spinney claims that Spinney's technique requires on average two reads, with a worst case of four reads, as can be seen for example, in Spinney's abstract. Michels' approach of two search engines (one with a subset of the lookup table) cannot improve on the two read performance of Spinney's system. Accordingly, one of ordinary skill in the art would not be motivated to combine Spinney with Michel to try to improve the speed of operation, while adding to the cost and circuit board space that Spinney was trying to reduce.

Accordingly, it is respectfully submitted that the combination of Spinney and Michels does not disclose or suggest all of the elements of the claimed invention, and that even if the combination did (not admitted), one of ordinary skill in the art would not find motivation, teaching, or suggestion to combine the references. Therefore it is respectfully requested that this rejection be withdrawn.

In view of the above amendments and remarks, it is respectfully submitted that each of claims 1-21 recite subject matter that is neither disclosed nor suggested in the cited prior art. It is therefore respectfully requested that claims 1-21 be allowed, and that this application be passed to issue.

In the event this paper is not being timely filed, Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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